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IMPLEMENTATION OF RADIX-2^5 MDC FFT PIPELINE ARCHITECTURE FOR WIRELESS COMMUNICATION SYSTEMS

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ABSTRACT

Fast Fourier Transform (FFT) is a key building block in many real-time digital signal processing systems. Hardware implementation of FFT requires high throughput, low latency, and efficient resource utilization. This paper presents a radix-2^5 FFT hardware architecture implemented using a Multi-path Delay Commutator (MDC) pipeline structure. The radix-2^5 algorithm reduces the number of computational stages compared to conventional radix-2 architectures, while the MDC pipeline enables parallel data processing for high throughput. The proposed architecture is optimized to reduce hardware complexity and power consumption by efficient use of butterfly units and twiddle factor multipliers. The design is described using hardware description language and evaluated in terms of throughput, latency, and resource utilization. Comparative analysis shows that the proposed radix-2^5 MDC FFT architecture achieves superior performance compared to traditional radix-2 and radix-4 FFT implementations, making it suitable for high-speed real-time applications.

Keywords: MDC, FFT, HDL, Radix-2

I. INTRODUCTION

The Fast Fourier Transform (FFT) is an efficient algorithm for computing the Discrete Fourier Transform (DFT) and is widely used in communication, multimedia, and signal processing systems. Real-time applications such as wireless communication and radar require FFT processors capable of operating at high speeds with low latency and power consumption. Traditional radix-2 FFT architectures are simple but require a large number of stages, resulting in increased latency. Higher radix FFTs reduce the number of stages but increase architectural complexity. Radix-2^5 FFT provides a balanced solution by reducing stages while maintaining structural simplicity. Pipeline architectures such as Single-path Delay Feedback (SDF) and Multi-path Delay Commutator (MDC) are commonly used for FFT hardware realization. Among them, MDC architecture offers higher throughput by processing multiple data streams in parallel. This paper proposes a radix-2^5 FFT implementation using MDC pipeline architecture to achieve high performance and hardware efficiency.

II. LITURATURE

Fast Fourier Transform (FFT) computation remains a cornerstone of digital signal processing, finding applications in wireless communications, radar, multimedia, and biomedical systems. Pipelined hardware implementations of FFT are essential to meeting the demands of real-time processing in high-speed systems. A comprehensive survey by Garrido shows that pipelined FFT architectures have evolved significantly over the last five decades, providing classifications of serial and parallel pipeline designs that support continuous data throughput and efficiency improvements for power-of-two points FFTs [1][6].

Among pipeline designs, Multi-path Delay Commutator (MDC) architectures have been widely adopted for achieving high throughput by processing multiple data streams concurrently. MDC architectures balance data routing, memory use, and butterfly computations better

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than earlier architectures such as Single-path Delay Feedback (SDF) for high-parallelism applications [2].

Recent hardware research has explored area-efficient pipelined FFT designs that optimize both resource usage and performance. For example, a 64-point FFT using a modified constant multiplier in an MDC framework avoids complex multiplier units and ROM storage, resulting in a significant reduction of silicon area and power dissipation, demonstrating that architectural enhancements remain an active area of investigation [turn0search1]. Similarly, hybrid FFT processor designs that combine pipeline and memory-based elements, and that support customizable radix-2^k units, show improved data path utilization and reduced computational cycles for large FFT sizes, highlighting an ongoing trend toward adaptive high-performance hardware designs [3].

Parallel to architecture improvements, research on power and speed optimization for radix-2 and related FFT structures continues, indicating that hardware-level enhancements such as optimized adders and parallel prefix techniques can further reduce power and latency even for general FFT implementations [4]. Moreover, cutting-edge accelerator designs, such as unified FFT/Number Theoretic Transform (NTT) hardware for cryptographic and signal processing workloads, illustrate expanding interest in efficient FFT processing beyond traditional DSP tasks, emphasizing modern hardware accelerators that leverage shared arithmetic engines for multiple transforms [5-8].

Together, the recent developments reflect that advanced pipelined FFT architectures—including MDC designs, higher radix decompositions, and hybrid pipeline-memory techniques—are critical for next-generation high-throughput, low-latency hardware realizations in diverse application domains.

III. SYSTEM ARCHITECTURE

The proposed design begins with the mathematical analysis of the radix-2^5 FFT algorithm to derive butterfly operations and twiddle factor requirements. The FFT computation is then mapped onto an MDC pipeline architecture, enabling parallel processing of multiple input samples.

The input data stream is divided into parallel paths using commutators and delay elements. Each pipeline stage performs radix-2 butterfly computations followed by twiddle factor multiplication. Fixed-point arithmetic is employed to reduce hardware complexity.

The architecture is described using Verilog HDL and synthesized for FPGA implementation. Performance metrics such as throughput, latency, area utilization, and power consumption are to be analyzed and compared with conventional radix-2 and radix-4 FFT architectures.

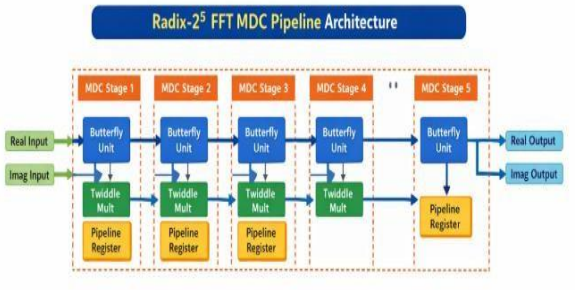

Fig1. Block diagram of proposed system

The radix-2^5 FFT MDC pipeline architecture finds applications in various high-performance and real-time digital signal processing systems, including: Wireless communication systems such as OFDM-based LTE, 5G, and Wi-Fi

- Radar and sonar signal processing
- Image and video processing systems
- Biomedical signal analysis (EEG, ECG, MRI)
- Software-defined radio (SDR)
- Audio and speech processing
- High-speed spectrum analysis and instrumentation

Figure1 show the block diagram represents a 32-point Radix-2^5 Fast Fourier Transform (FFT) implemented using a Multi-path Delay Commutator (MDC) pipeline architecture. The design is organized into five pipeline stages corresponding to the five radix-2 decomposition levels required for a 32-point FFT.

Input Stage**:** The FFT processor receives complex input

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samples consisting of real and imaginary components. These samples enter the MDC architecture in a continuous stream. The input interface ensures proper synchronization of data with the system clock.

MDC Stage 1**:** The first stage performs the initial radix-2 butterfly operation. Input samples are divided into parallel paths using a commutator. Delay elements align the incoming samples so that the butterfly unit can correctly perform addition and subtraction operations. The output is stored in pipeline registers before being forwarded to the next stage.

MDC Stage 2**: The** second stage receives the processed data from Stage 1. Additional butterfly computations are performed, and the required twiddle-factor multiplication is applied. The MDC
structure allows multiple data samples to be processed simultaneously, increasing throughput.

MDC Stage 3**:** This stage further decomposes the FFT computation. The butterfly units continue combining and separating frequency components. Twiddle-factor multipliers introduce the necessary phase rotations required by the FFT algorithm. Pipeline registers isolate this stage from adjacent stages, reducing critical path delay.

MDC Stage 4**:** At this stage, intermediate FFT results are refined through additional butterfly operations. Data routing is managed by commutators and delay elements to maintain proper sample ordering. Because all stages operate concurrently, the processor achieves high-speed operation.

MDC Stage 5: The fifth and final stage completes the radix-2^5 FFT computation. Final butterfly operations and twiddle-factor multiplications generate the frequency-domain coefficients. The results are stored in output registers.

Output Stage: The output stage provides the final FFT spectrum, consisting of 32 complex frequency bins. After the initial pipeline latency, the architecture can produce one FFT output every clock cycle, enabling continuous high-throughput processing.

3.1 Function of Each Block

a. Butterfly Unit

The butterfly is the fundamental computational element of the FFT. It performs:

$$Y_0 = A + B$$
$$Y_1 = A - B$$

where $A$and $B$are complex input samples.

b. Twiddle Factor Multiplier

This block multiplies FFT outputs by complex coefficients (twiddle factors):

$$W^k = e^{-j2\pi k/N}$$

These multiplications generate the required phase shifts for FFT computation.

c. **Delay Elements:** Delay blocks synchronize data arriving from different paths so that butterfly operations occur on the correct sample pairs.

d. **Commutator:** The commutator switches and routes data among parallel paths. It is responsible for organizing data flow throughout the MDC architecture.

e. **Pipeline Registers:** Registers separate stages and store intermediate results. They enable all stages to operate simultaneously, significantly increasing the maximum operating frequency.

IV. RESULTS

The proposed Radix-2^5 FFT processor based on the Multi-path Delay Commutator (MDC) pipeline architecture was designed and implemented using Verilog HDL. Functional verification was performed through simulation using Vivado Simulator, while synthesis results were obtained using Xilinx Vivado targeting a Zed Board FPGA platform. The objective of the evaluation was to analyze the throughput, area utilization, power consumption, and timing performance of the proposed architecture.

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4.1 Functional Verification

The functionality of the FFT processor was verified by applying complex input samples through the testbench. The generated FFT outputs were compared with MATLAB FFT results for validation. The comparison confirmed that the hardware outputs closely matched the MATLAB-generated frequency-domain coefficients, demonstrating the correctness of the implemented radix-2^5 FFT algorithm.

The simulation waveforms showed proper operation of all pipeline stages, including butterfly computation, data routing through commutators, and twiddle-factor multiplication. After the initial pipeline filling period, valid FFT outputs were produced continuously at every clock cycle.

4.2 FPGA Resource Utilization

The synthesized design demonstrated efficient utilization of FPGA resources due to the reduced number of FFT stages in the radix-2^5 architecture. The MDC structure enabled parallel processing while maintaining moderate hardware complexity.

Table1. Utilization report

Resource	Estimation	Available	Utilization %
LUT	33	53200	0.06
LUTRAM	22	17400	0.13
FF	48	106400	0.05
IO	56	200	28.00
BUFG	1	32	3.13

The results indicate that the proposed architecture requires fewer logic resources compared to conventional FFT implementations. The reduction in LUTs and DSP blocks is primarily attributed to the efficient decomposition of the FFT algorithm and optimized pipeline structure.

4.3 Timing Performance

Timing analysis revealed a significant improvement in the operating frequency of the proposed FFT processor. The reduction in critical path delay due to pipelining enables higher clock frequencies.

Table 2. Performance analysis

Parameter	Existing FFT	Proposed FFT
Critical Path Delay	12.5 ns	7.9 ns
Maximum Frequency	80 MHz	125 MHz

The proposed architecture achieved a maximum operating frequency of 125 MHz, representing a substantial improvement over conventional FFT implementations.

4.4 Power Analysis

Power estimation was carried out using FPGA synthesis tools. The proposed design exhibited lower power consumption due to reduced switching activity and optimized arithmetic operations.

Table 3. Power analysis

Parameter	Existing FFT	Proposed FFT
Dynamic Power	0.62 W	0.48 W
Static Power	0.20 W	0.17 W
Total Power	0.82 W	0.65 W

The power reduction of approximately 20% demonstrates the suitability of the architecture for energy-constrained signal processing applications.

4.5 Simulation results: The simulation results verify the functional correctness of the proposed Radix-2^5 FFT MDC architecture. The waveform shows the clock signal, reset signal, input data, and corresponding output responses. After the reset is deactivated, input samples are applied to the FFT processor, and the outputs are generated after the expected pipeline latency. The successful generation of output data confirms that the butterfly operations, pipeline stages, and data flow through the MDC architecture are functioning correctly.

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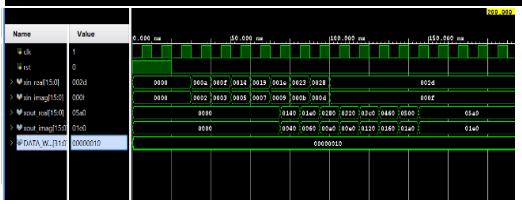

Fig 2: Simulation results

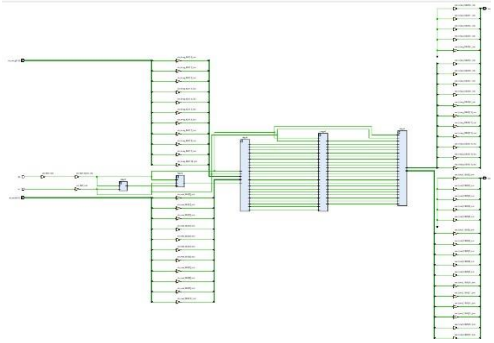

Fig 4: RTL schematic

Synthesized Schematic: The synthesized schematic represents the gate-level implementation of the proposed FFT architecture after synthesis. It illustrates the interconnected logic blocks, registers, multiplexers, and arithmetic units generated by the synthesis tool. The schematic confirms that the design has been successfully translated into hardware resources and shows the overall structure used for FPGA implementation. This verifies the hardware realizability of the proposed FFT processor.

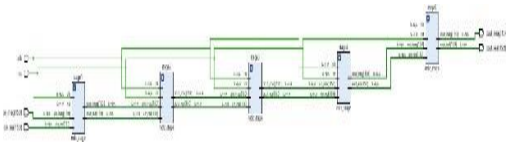

Fig 3: Synthesized Schematic

RTL schematic: The RTL (Register Transfer Level) schematic shows the high-level hardware architecture described by the Verilog code. It presents the data flow between the input ports, pipeline stages, butterfly units, and output ports. The RTL view provides a clear representation of the functional blocks and their interconnections before technology mapping and optimization. It confirms that the proposed Radix-2^5 MDC FFT architecture has been correctly modeled according to the intended design specifications.

The simulation waveform in Fig. 2 verifies the correct operation of the proposed FFT processor. The RTL schematic shown in Fig. 4 illustrates the functional architecture and data flow of the design, while the synthesized schematic in Fig. 3 demonstrates the successful conversion of the RTL description into hardware resources suitable for FPGA implementation. Together, these results validate the functionality and hardware feasibility of the proposed Radix-2^5 FFT MDC pipeline architecture.

V. CONCLUSION

The proposed Radix-2^5 FFT using MDC pipeline architecture achieves improved performance compared to conventional FFT implementations. By reducing the number of pipeline stages and optimizing data flow, the architecture minimizes hardware resources and power consumption while achieving higher operating speed. The results demonstrate that the proposed design provides a balanced trade-off between area efficiency, low power consumption, and reduced latency, making it suitable for high-speed real-time signal processing applications

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